DELAY ESTIMATION MODEL FOR HIGH SPEED INTERCONNECTS IN VLSI

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Abstract: In recent days there is huge demand for high speed VLSI networks. In order to judge the behavior of on-chip interconnects the coupling capacitances and interconnect delays plays a major role. As we switch to lower technology there is on-chip inductance effect that leads to interconnect delay. In this paper we try to apply second order transfer function designed with finite difference equation and Laplace transform at the source and load termination ends. Analysis shows that current mode signaling in VLSI interconnects provides times better delay performance than voltage mode.

Keywords: Current Mode, Voltage Mode, VLSI Interconnect

I. INTRODUCTION

As the number of transistors on a chip continues to increase, on-chip communication becomes a more important facet of architectural design. Traditional electrical wires, typically driven by digital components using simplistic digital signals have issues to address in the scaling chip multiprocessor market, specifically latency and energy. Global wire latency remains relatively constant, translating to a larger relative latency for even moderately-sized systems. In order to ensure signal quality, digital repeaters and packet-switching routers must be added to facilitate the transmission of long distance communications, contributing further to the latency and energy issues. Current research focuses on a few categories of solutions, each with unique benefits and limitations. The current convention is the use of packet-switching networks topologies to provide the interconnect backbone for chip-multiprocessors. A packet-switched network-on-chip (NoC) provides in-field scalability, the ability to use commercial-off-the-shelf components, and high aggregate throughput. However, a NoC also requires higher power routers and potentially long latencies for long distance communication. Another state-of- the-art solution for interconnects uses on- chip optics. Research is currently being proposed to use either waveguides or free- space optics to provide a high-throughput, low-energy, low-latency medium for on- chip communication. On the other hand, optics also has issues that prohibit its immediate use as an interconnect backbone.

First, current optical components are not easy to integrate into standard silicon CMOS process, making it more difficult to fabricate with the current technologies without sacrificing electro-optical conversion efficiency. Additionally, while some on-chip lasers exist, most often, off-chip lasers are used to provide the optical power, shifting the onus of energy efficient operation off-chip, but not removing it from the system.

II. RELATED WORKS

Signaling in global strains is a main bottleneck in excessive performance VLSI systems because of the dominant problem of signal propagation delays in comparison to circuit delays. So, correct and accurate delay estimation models are required in cutting-edge-mode signaling. Accurate estimation of propagation delay in worldwide interconnects plays a main place in the early design levels of VLSI systems compared to neighborhood interconnect delays because, global wires supports predominant

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capabilities like clock, sign distribution among the useful blocks and affords power/ground to all functions on a chip. Starting from lumped RC model to distributed RLC version, diverse techniques [6]-[8] based on analytical closed form formulations had been proposed to model delay in voltage- mode interconnects. Similarly for modern- day-mode RC interconnects, closed-form delay analysis version becomes presented in [9] and the evaluation does not encompass the fast aspect input reaction. In [10] closed-form delay model for allotted contemporary-mode RC line is provided, which included the practical rapid edge input reaction issue but this version should now not include the inductance impact in present day-mode

interconnect. A delay estimation model[11], that's derived the use of the concept of soaking up inductance impact into equal RC version, then changed nodal evaluation (MNA) become used. Various closed-form delay models [9]-[13] for on-chip interconnects in present day-mode signaling have more inaccuracy in phrases of postpone estimation.

III. FINITE DIFFERENCE EQUATION AND LAPLACE TRANSFORM

The Taylor series expansion for a function of one variable about the point x is

$$f(x+h) = f(x) + h\,f'(x) + \frac{h^2}{2!}f''(x) + O(h^3)$$

…….. (1)

The notation O(h3) indicates that the series, when truncated at the quadratic term in h, contains errors that scale as h3 and higher powers of h.

We can immediately obtain an approximation to the derivative of f(x) from the first two terms of the expansion.

$$f'(x) = \frac{f(x+h) - f(x)}{h} + O(h^1) \text{..... (2)}$$

Note that, even though we neglect terms of O(h2) in the expansion, since we divide through by h to obtain the derivative expression the approximation is correct to O(h1) only. Note that there is an asymmetry in this approximation to the derivative at x, since the function at x and x+h occur, but not the function at x-h. This is therefore referred to as a forward difference approximation. It is possible to expand f(x) in the negative direction in the Taylor expansion and hence to obtain a backward difference approximation

$$f(x-h) = f(x) - h\,f'(x) + \frac{h^2}{2!}f''(x) + O(h^3)$$

…….. (3)

$$f'(x) = \frac{f(x) - f(x-h)}{h} + O(h^1) \text{..... (4)}$$

By combining forward and backward difference approximations it is possible to obtain a central difference approximation to the derivative of f(x) at x that contains errors of order O(h2) . Note the difference

in scaling of errors for the central difference approximation when compared with the forward and backward difference approximations.

$$f(x+h) = f(x) + h\,f'(x) + \frac{h^2}{2!}f''(x) + O(h^3)$$

$$f(x-h) = f(x) - h\,f'(x) + \frac{h^2}{2!}f''(x) + O(h^3)$$

$$f(x+h) - f(x-h) = 2h\,f'(x) + 2\frac{h^3}{3!}f''(x) + O(h^4)$$

$$f'(x) = \frac{f(x+h) - f(x-h)}{2h} + O(h^2)$$

…….. (5)

By retaining terms in the Taylor series to order h3 we can obtain an approximation for the second derivative which contains errors of order h2

$$f(x+h) = f(x) + h\,f'(x) + \frac{h^2}{2!}f''(x) + \frac{h^3}{3!}f'''(x) + O(h^4)$$

$$f(x-h) = f(x) - h\,f'(x) + \frac{h^2}{2!}f''(x) - \frac{h^3}{3!}f'''(x) + O(h^4)$$

…….. (6)

Add these expansions to obtain

$$h^2 f''(x) = f(x+h) - 2\,f(x) + f(x-h) + O(h^4)$$

$$f''(x) = \frac{f(x+h) - 2\,f(x) + f(x-h)}{h^2} + O(h^2)$$

…….. (7)

A. Taylor series expansions in more than one dimension

A PDE contains at least two independent variables and so we need to approximate differential operators in at least two dimensions. This is done using Taylor series expansions in more than one dimension. Suppose

$u = u(x,y)$ (8)

The Taylor series expansion of u about the point (x,y) is The vector notation for this expansion is

$$u(x+h, y+k) = u(x,y) + h\,u_x(x,y) + k\,u_y(x,y) + \frac{h^2}{2!}u_{xx}(x,y) + \frac{2hk}{2!}u_{xy}(x,y) + \frac{k^2}{2!}u_{yy}(x,y) + O(|\mathbf{h}|^3)$$

$$\mathbf{h} = \begin{pmatrix} h \\ k \end{pmatrix}$$

…….. (9)

$$u(\mathbf{x}+\mathbf{h}) = u(\mathbf{x}) + \mathbf{h}^T . \nabla u(\mathbf{x}) + \frac{1}{2!}\mathbf{h}^T . \nabla\nabla u(\mathbf{x}) . \mathbf{h} + O(|\mathbf{h}|^3)$$

$$\mathbf{h} = \begin{pmatrix} h \\ k \end{pmatrix} \quad \mathbf{h}^T =$$

$$(h \quad k)\,\mathbf{x} = \begin{pmatrix} x \\ y \end{pmatrix} \quad \nabla\nabla = \frac{\partial^2}{\partial x_i \partial x_j}$$

…….. (10)

Returning to the long-hand notation, the expansion of u(x,y) in the x direction is

$$u(x+h, y) = u(x,y) + h\,u_x(x,y) + \frac{h^2}{2!}u_{xx}(x,y) + O(h^3)$$

$$u(x-h, y) = u(x,y) - h\,u_x(x,y) + \frac{h^2}{2!}u_{xx}(x,y) + O(h^3)$$

…….. (11)

If we subtract these two equations and rearrange to make ux the subject of the equation we find that the central difference approximation to ux is

$$u_x(x,y) = \frac{u(x+h, y) - u(x-h, y)}{2h} + O(h^2)$$

…….. (12)

We can also obtain forward and backward difference approximations which contain errors of order O(h1) from the Taylor series expansion in either direction. It is convenient to write the function u at points

on a grid for numerical solution with subscripted indices rather than arguments. Thus we make the equivalence

$$u(x, y+k) = u_{i+1,j} \text{.....} (13)$$

k is the step size or distance between gridpoints in the y direction in the numerical solution.

Perversely, Farlow reverses the order of the arguments/indices in going over to the gridpoint index. We will do the same to maintain consistency

with Farlow. The indicial representation of the first and second order partial derivatives is given below and illustrated by corresponding 'computational molecules'.

$$u_x(x,y) = \frac{1}{2h}\left(u_{i,j+1} - u_{i,j-1}\right) + O(h^2)$$

$$u_y(x,y) = \frac{1}{2k}\left(u_{i+1,j} - u_{i-1,j}\right) + O(k^2)$$

$$u_{xx}(x,y) = \frac{1}{h^2}\left(u_{i,j+1} - 2u_{i,j} + u_{i,j-1}\right) + O(h^2)$$

$$u_{yy}(x,y) = \frac{1}{k^2}\left(u_{i+1,j} - 2u_{i,j} + u_{i-1,j}\right) + O(k^2)$$

…….. (14)

Provided that the step sizes in the two directions (h and k) are equal, then we obtain the following approximation for the Laplacian operator in 2 dimensions.

$$\nabla^2 u(x,y) = \frac{1}{h^2}\left(u_{i+1,j} + u_{i-1,j} + u_{i,j+1} + u_{i,j-1} - 4u_{i,j}\right) + O(h^2)$$

…….. (15)

Voltage mode interconnects

Voltage mode signaling is most widely used in VLSI chips. In voltage mode signaling, receiver provides high input impedance (ideally infinity). The information is conveyed in the form of voltage. The output voltage is a function of input signal and is varied according to supply voltage. Fig.1 shows the theoretical model of conventional voltage mode interconnect implementation [5]. The output is terminated by an open circuit.

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CMOS representation of voltage mode is shown in Fig. 2 [1, 3]. The driver consists of an inverter which drives long RC interconnect chain. This is terminated by high input impedance of the inverter circuit at the receiver. This high input impedance of the receiver gives rise to high input capacitance which leads to high charging and discharging time for RC interconnect chain. Hence voltage mode signaling has large delay. Due to high input impedance at the receiver, the charge accumulated at the input of the receiver does not get effective discharge path to ground as a result this may cause electrostatic induced gate oxide break down.

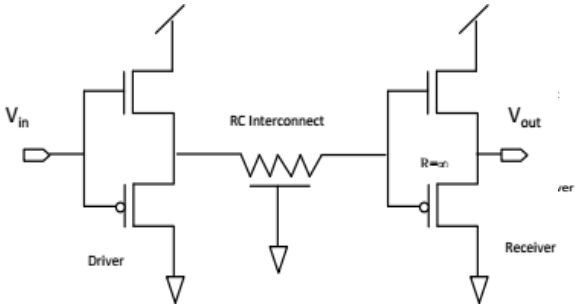


Fig. 2. CMOS representation of voltage mode signaling [5].

Current mode interconnects

In current mode signaling, information is represented as current signal. The receiver provides low impedance (ideally zero) at its input. In current mode signaling line is terminated by shorting the wire. The theoretical modelofcurrent mode signaling is as shown in Fig. 3 [5]

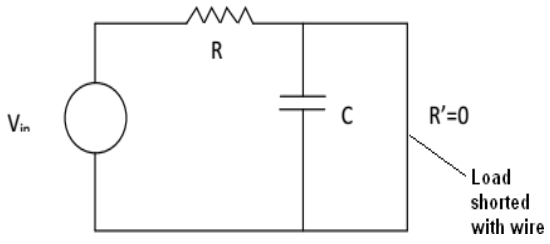


Fig. 3. Current mode signaling

The CMOS representation of current mode signaling is shown in Fig. 4. The receiver senses current signal at its input and provides low impedance.

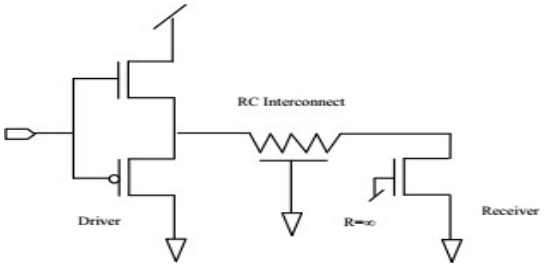
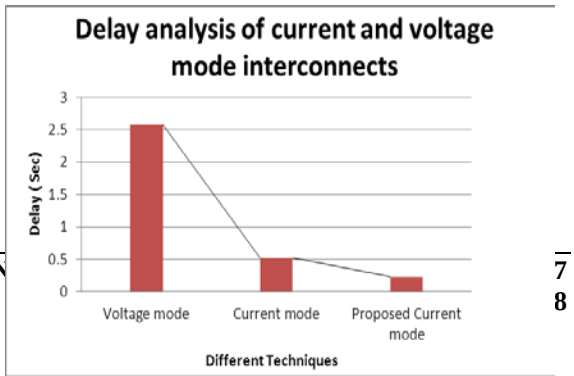


Fig. 4. CMOS representation of current mode signaling [5]

Table I Delay Analysis for voltage and Current Mode Interconnects [13, 14].

Signaling mode	Delay (ns)	P Total) (µw)
Voltage mode	2.58	22.01
Current mode	0.520	115.08
Proposed Current mode	0.010	19.33

Table I shows the delay analysis for both voltage and current mode interconnects [13-14]. It is analyzed that with Proposed Current mode interconnects delay decreases from 2.58ns to 0.010ns however power dissipation in the circuit increases from 22.01µw to 19.33µw. This is due to the low impedance at the receiver of current mode interconnect circuit. The overall figure of merit power-delay- product (PDP) of current mode increases. This displays the improved performance and advantage of current mode over voltage mode interconnects. The delay analysis for current and voltage mode interconnect is shown in Fig. 10. It is seen that there is 79.84% reduction in current mode



interconnect delay.

IV. CONCLUSION

This paper presents second order transfer function designed with finite difference equation and Laplace transform at the source and load termination ends current mode signaling for delay estimation of current mode high speed VLSI interconnects. The perseverance of the current study is to estimate the delay of current-mode VLSI interconnects and to find the interaction between delay for various lengths, line inductances and load capacitances using existing voltage mode. All the benefits give current mode signaling an upper edge over the voltage mode signaling. At highly miniaturized technologies, interconnects with current mode signaling would be the best choice with the assistance of HSPICE tool.

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